Notice of Allowability	Application No.	Applicant(s)	
	09/872,091	ARAYA ET AL.	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *September 25, 2007*.

2. ☒ The allowed claim(s) is/are *11-26*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Introduction

1. This communication is in response to the Applicants' communication dated September 25, 2007. Claims 11-16 and 20-22 were amended. Claims 11-26 of the application are pending.

Examiner's Amendment

2. Authorization for this examiner's amendment was given in a telephone conversation by Ms. Katherine Vieyra on November 13, 2007.

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to the applicants, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

3. In the claims:

In claim 11, line 7, "an architecture design"

has been changed to

-- the architecture design --.

In claim 11, lines 16-17, "based on a result of an implementation"

has been changed to

-- based on an implementation --.

In claim 13, line 2, "with respect to a processing rate"

has been changed to

-- using a processing rate --.

In claim 14, line 3, "a high-level design stage"

has been changed to

-- the high-level design stage --.

In claim 16, lines 8-12, "structuring the source code into elements representing at least one of the hardware units and the software units for use in the architecture design by compiling said source code;

calculating the data transfer rate on the bus by executing the compiled source code elements in a simulation program;

calculating bus traffic with regard to a given processing rate of the bus; and"

has been changed to

-- structuring the source code into elements representing the hardware units and elements representing the software units in the architecture design and compiling said source code;

organizing the compiled source code elements in a simulation program, executing the simulation program and calculating the data traffic on the bus;

calculating bus traffic using a known processing rate of the bus; and--.

In claim 17, lines 4-5, "the number of times in effecting data transfer on the bus is multiplied by n/m and is then divided by the processing rate"

has been changed to

-- the data traffic on the bus is multiplied by n/m and is then divided by the processing rate of the bus --.

In claim 18, line 1, "The method according to any one of the preceding claims"

has been changed to

-- The method according to claim 11--.

In claim 20, line 2, "evaluating and facilitating an architecture design"

has been changed to

-- facilitating and evaluating an architecture design --.

In claim 20, lines 7-8, "creating an architecture design"

has been changed to

-- creating the architecture design --.

In claim 20, line 9, "for evaluating data transfer that occurs"

has been changed to

-- for counting data traffic that occurs --.

In claim 20, line 11, "effects said data transfer"

has been changed to

-- effects data transfer --.

In claim 20, lines 16-17, "the variables defined in advance is written"

has been changed to

-- the variables defined in advance are written --.

In claim 20, lines 22-27, "simulating said modified source code elements at the high level design stage and evaluating said data transfer on the bus, comprising the steps of:

compiling said structured source code elements;

executing the compiled source code elements on a simulation platform;

calculating the bus traffic based on the number of times in effecting of data transfers according to the evaluation function and a known processing rate of the bus"

has been changed to

-- compiling said structured source code elements;

organizing the compiled source code elements in a simulation program;

executing the simulation program and calculating the data traffic on the bus according to the evaluation function at the high level design stage;

calculating the bus traffic based on the data traffic and a known processing rate of the bus--.

In claim 20, lines 32-34, "by starting with changing said bus configuration and restructuring the source code, and wherein said performance evaluation is used to modify the architecture design of the LSI"

has been changed to

-- by starting with restructuring the source code and changing said bus configuration --.

In claim 21, line 3, "at a high-level design stage"

has been changed to

-- at the high-level design stage --.

In claim 24, lines 3-5, "the number of times in effecting data transfer on the bus is multiplied by n/m and is then divided by the processing rate"

has been changed to

-- the data traffic on the bus is multiplied by n/m and is then divided by the processing rate of the bus --.

In claim 26, lines 1-2, "the evaluation function is to increment a counting value"

has been changed to

-- the evaluation function increments a counter value --.

A clean copy of allowed claims is included.

Reasons for Allowance

4. Claims 11-26 of the application are allowed over prior art of record.

5. The following is an Examiner's statement of reasons for the indication of allowable subject matter:

The closest prior art of record shows:

(1) a set of tools for design space exploration, HW/SW co-design, co-simulation and cosynthesis of embedded systems; starting a design from a common initial executable description and then partition it into HW and SW components on the basis of execution time and time spent in communicating between HW and SW partitions; C/C++ language is used for modeling the system behavior, due to great flexibility offered and availability in every platform; data for partitioning is derived by profiling the source code; a standard execution time profiler and a data transfer profiler are used; a master-slave type relation is used between HW/SW units; the HW/SW cosynthesis finds a trade-off between HW and SW while satisfying various constraints; profiling functions are inserted into an executable code; during data transfer, for each variable access, a call to a counter function is made, which logs the access of the variable; when the program exits, the logged file is read and interpreted by an estimator; the algorithm finds a solution that gives the highest system speed up without increasing the system bus load to unacceptable level; the bus load is minimized by the partitioner; the HW/SW co-simulation is achieved using a set of C functions which implement communication between HW and SW (**Tamemae et al.,** "AKKA: A tool-kit for cosynthesis and prototyping", IEE, UK, 1996);

(2) a method and apparatus for determining test coverage estimation for an electronic circuit using a high level description and a processing unit; the processing unit (CPU) accesses the description and parses it to allow generation of new code; the new code can be used to simulate the electronic circuit and to collect test coverage information; the system uses profiling

which is a practice of surrounding existing computer code of high level language program with monitor code; profiling is same as instrumenting the high level language program; profiling techniques are used for generation of additional code to check for occurrence of various events; the method begins by parsing the original high level language description having executable assignment statements; a new high level language description including new code generated and the original high level description is generated; the new high level language description has a plurality of new assignment statements to store in a file whether at least one variable on the right side of each assignment statement has been set to a predetermined value, whether the left side of each assignment statement has been set to a predetermined set of values and whether each assignment statement in the plurality of assignment statements has been executed; the output file is used by the CPU to create a test coverage information (**Raimi,** U.S. Patent 5,604,895); and

(3) a method and system for designing a circuit including a plurality of pre-designed circuit blocks; the method includes bus planning involving translating the front-end specifications into top-level bus specifications; the method starts with a high-level functional model of the system being designed; the designer constructs a high level diagram of the bus structure for the design; the designer has a rough idea of the traffic on each buses and estimates how many buses and what capacity are needed; buses are designed to meet the required system performance while minimizing interface logic; the designers use this architecture to create a bus functional model to verify that the design operates as defined in the specification; simulation tools are used in bus design to test the bus components; the simulation tools include models written in Verilog and/or VHDL (**Chang et al.,** U.S. Patent 6,269,467).

None of these references taken either alone or in combination with the prior art of record discloses a method in a LSI design and development process for creating and evaluating an architecture design for an algorithm design by performing a performance evaluation of at least one bus at a high-level stage of said design and development process, specifically including:

(Claim 11) "determining whether the source code is to be modified based on whether a line of source code represents writing data to variables that are defined in advance and are loaded onto the bus to be evaluated;

modifying at least one element of said source code based on an implementation of said evaluation function".

None of these references taken either alone or in combination with the prior art of record discloses a method in a LSI design and development process for facilitating and evaluating an architecture design for an algorithm design by performing a performance evaluation of at least one bus at a high-level stage of said design and development process, specifically including:

(Claim 20) "determining whether a line of source code represents writing data to variables that are defined in advance and are loaded onto the bus to be evaluated;

upon the determination, modifying the source code by embedding the evaluation function just before or after the line of source code in which one or more of the variables defined in advance are written;

repeating the steps of sequentially reading in the source code, determining whether the source code represents writing data to variables defined in advance, and modifying the source

code by embedding the evaluation function until the source code is completely read in and modified up to a last line of source code".

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez, can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K. Thangavelu
Art Unit 2123
November 13, 2007